Claims

What is claimed is:

1. An integrated circuit device, comprising:

a peripheral region and a core region;

wherein the peripheral region comprising one or more electrostatic discharge protection transistors;

the electrostatic discharge protection transistors comprising a field effect transistor, a source region, and a drain region;

the source and drain regions comprising lightly doped and heavily doped areas of a semiconductor;

the heavily doped areas being spaced apart from a channel region of the field effect transistor and having a dopant concentration of at least about $1x10^{18}$ atoms per cm^3.

2. The device of claim 1, wherein the channel region is less than or equal to about 1.0 μm in length.

3. The device of claim 2, wherein the channel region is less than or equal to about 0.3 μm in length.

4. The device of claim 1, wherein the heavily doped areas have a dopant concentration of at least about $1x10^{19}$ atoms per cm^3.

5. The device of claim 4, wherein the heavily doped areas have a dopant concentration of at least about $5x10^{19}$ atoms per cm^3.

6. The device of claim 1, wherein the field effect transistor comprises an insulating layer having a thickness less than or equal to about 80 Å.

7. The device of claim 1, wherein the integrated circuit device is a flash memory device.

8. The device of claim 7, wherein the flash memory device comprises a virtual ground array structure and SONOS type memory cells.

9. A method of forming an integrated circuit device, comprising:

providing a semiconductor substrate having a core region and a peripheral region;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, heavily doping source and drain regions for the electrostatic discharge protection transistors.

10. The method of claim 9, wherein a portion of the other transistors are of the same type as the electrostatic discharge protection transistors and are unmasked while heavily doping source and drain regions for the electrostatic discharge protection transistors.

11. The method of claim 10, wherein the heavy doping would cause a short channel effect in the electrostatic discharge protection transistors were it not for the spacers.

12. The method of claim 9, wherein the integrated circuit device is a flash memory device.

13. The method of claim 12, wherein the flash memory device comprises a virtual ground array structure and SONOS type memory cells.

14. The method of claim 13, wherein the flash memory device comprises word lines spaced apart by about 1 μm or less.